REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicants thank the Examiner for carefully considering the present application.

Disposition of Claims

Claims 1-16 are currently pending in the present application. Claims 1, 7, 12, and 16 are independent. The remaining claims depend, directly or indirectly, from any one of claims 1, 7, and 12.

Claim Amendments

Claims 1, 7, 12, and 16 have been amended in this reply to clarify the present invention recited. These amendments are fully supported by, for example, Fig. 1 of the original application. Accordingly, no new matter has been added by these amendments.

Rejection(s) Under 35 U.S.C § 103

Claims 1-4, 6-10, and 12-16

Claims 1-4, 6-10, and 12-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,611,042 (hereinafter "Lordi"). For the reasons set forth below, this rejection is respectfully traversed.

Independent claim 1, as amended, recites a random access memory having a data error detection and correction mechanism. Specifically, claim 1 includes the limitations of "an error checking circuit operatively connected to receive data read from only the first

memory bank," and "the error checking circuit is electrically disposed between the first memory bank and the multiplexer."

Lordi, in contrast, does not disclose the limitations as recited in claim 1. As described in Lordi, the parity bit P1 from SRAM 1 (10) and the parity bit P2 from SRAM 2 (11) are coupled to a parity select logic (50). Namely, the parity select logic (50) receives *two* parity bits P1 and P2 from the SRAMs 1 and 2 (10, 11) respectively. See, for example, col. 2, lines 50-52. To this end, the apparatus disclosed in Lordi needs to not only arrange wiring between the SRAM 2 (11) and the parity select logic (50) but also synchronize signals of the parity bits P1 and P2. Lordi intends to detect and correct data error by both parity bits P1 and P2, while Lordi does not consider problems such as complexity of silicon space and high-frequency noise due to increasing wiring. Lordi does not allow for the parity select logic (50) being disposed between SRAM 1 (10) and the multiplexer (40) at all. The claimed invention as a whole must be considered. See MPEP 2141.02. Accordingly, Lordi fails to disclose or suggest the limitations recited in claim 1.

On the other hand, in the present invention, the error checking circuit uses parity data from *only* the first memory bank not both of the first memory bank and the second memory bank. This allows the error checking circuit to be disposed between the first memory bank and the multiplexer. It is noted that the present invention, in part, takes an optimistic approach that write data duplicated into the secondary bank is employed without parity checking if the parity data from the first memory bank is bad. Unlike Lordi, the prevent invention does not require parity bits from both the first memory bank and the secondary memory bank. Further, those skilled in the art will recognize that Lordi must employ <u>two</u> parity checkers, one for each memory bank. On the other hand, by assuming

that the second memory bank will be good when the first is bad, the present invention avoids the use of a second parity checker. By way of this, advantageously, the prevent invention can solve the problems due to increasing wiring.

In view of above, Lordi fails to show or suggest the present invention as recited in independent claims 1 as amended. Also, independent claims 7, 12, and 16 include the similar limitations as recited in claim 1 as amended. Thus, independent claims 1, 7, 12, and 16 as amended are patentable over Lordi. Dependent claims are also allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Claims 5 and 11

Claims 5 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lordi in view of U.S. Patent No. 6,237,124 (hereinafter "Plants"). For the reasons set forth below, this rejection is respectfully traversed.

Plants fails to at least teach that which Lordi lacks. Plants is directed to a technique for detecting error in stored data. Specifically, Plants merely discloses in Figure 4 a cyclical redundancy checking (CRC) circuit (40) that checks for single event upset (SEU) occurrences on an output from a multiplexer (42) that inputs data read from an SRAM (located in FPGA core 10 as shown in Figure 5A). See Plants, column 4, lines 15-29. Thus, Plants does not disclose those limitations of "an error checking circuit operatively connected to receive data read from only the first memory bank," and "the error checking circuit is electrically disposed between the first memory bank and the multiplexer," as discussed above.

As mentioned above, Lordi does not disclose all of the limitations as recited claim 1. Plants fails to provide that which Lordi lacks. Claim 7 includes the similar limitations as

recited in claim 1. Thus, claims 1 and 7 are patentable over Lordi and Plants, whether considered separately or in combination. Claims 5 and 11 depend from either claim 1 or 7. Claims 5 and 11 are also patentable over Lordi and Plants for at least the same reasons. Accordingly, withdrawal of the rejection is respectfully requested.

Conclusion

The above amendments and remarks are believed to require no further prior art search. Also, Applicants believe that this reply is responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Because the amendments and remarks simplify the issues for allowance or appeal, and do not constitute new matter, entry and consideration thereof is respectfully requested.

Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226.053002; P5039).

Respectfully submitted,

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